

A Verilog-Based Double-Precision FPU: From Algorithmic Design to Hardware Verification

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Abstract: *Floating Point Units (FPUs) are essential components of modern processors and digital systems, enabling high-precision arithmetic operations required in scientific computing, signal processing, and embedded applications. This paper presents the design, simulation, and hardware implementation of an IEEE-754 compliant single-precision Floating Point Unit using Verilog HDL. The proposed FPU supports basic arithmetic operations such as addition, subtraction, multiplication, and division, along with exception handling and normalization mechanisms. The architecture is modular, enabling easy integration into larger processing systems. Functional verification is performed using Modalism, and hardware feasibility is demonstrated through synthesis results. The proposed design achieves accuracy, modularity, and efficient resource utilization, making it suitable for embedded and high-performance computing applications.*

Keywords: Floating Point Unit, IEEE-754, Verilog HDL, ModelSim, Arithmetic Logic Unit, Digital Design

