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FPGA-Based Real-Time 2D FIR Filter Implementation on DE10-Standard Board

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Abstract: *This paper presents the design, implementation, and validation of a 4×4 two-dimensional Finite Impulse Response (2D FIR) filter on an Intel Cyclone V FPGA development board (DE10-Standard). The architecture utilizes Verilog HDL with a pipelined convolution engine and a seven-state finite-state machine (FSM) for streaming data processing. Functional verification through RTL simulation in ModelSim and real-time hardware validation using Intel SignalTap Logic Analyzer confirm correct operation. Synthesis results demonstrate efficient resource utilization (< 5% logic elements, ~5% DSP blocks), timing closure at 108.6 MHz, and sustained throughput of ~10 M pixels/s. Bit-exact matching between simulation and hardware validates the design's correctness. The work demonstrates that FPGA-based 2D FIR filtering meets real-time constraints with minimal resource overhead, providing a scalable foundation for advanced image processing systems.*

Keywords: FPGA, 2D FIR filter, convolution, Verilog HDL, Cyclone V, FSM, pipelining, real-time image processing

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