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Design of An Automated Car Washing System with Verilog HDL

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Abstract: *Automation remains at the forefront of technological innovation, enabling the efficient control of processes without direct human involvement This project presents an advanced automated car washing system utilizing Field Programmable Gate Arrays (FPGAs) programmed in Verilog HDL.The system provides washing services that are rapid, convenient, and effective. A flow chart for controlling an automated car washing system with four working modes and implemented with a custom mode option is given. The resulting compact design minimizes power consumption and effectively addresses other major issues. These comprehensive optimizations meet stringent performance, area, and power requirements, elevating the operational efficiency of automated car washing systems. Furthermore, the design is synthesized and implemented using Xilinx's ISE Design Suite.*

Keywords: ISE Design Suite

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