IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429
Volume 5, Issue 10, June 2025
Impact Factor: 7.67

High Speed Low-Power Gate Level Synchronous Full Adder Designs

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Abstract: *In modern VLSI design, the full adder remains a fundamental component, directly influencing the overall efficiency of arithmetic circuits. This paper presents novel high-speed gate-level synchronous full adder designs that significantly optimize critical performance parameters including area, delay, and power consumption. Existing full adder implementations using AND-OR logic, half adders, and 2:1 multiplexers exhibit higher transistor counts (up to 74), increased delay (up to 20.03 ns), and elevated power dissipation (up to 137.5 µW). In contrast, the proposed designs—XAC, XNM, and XNAIMC—demonstrate remarkable improvements. The XNM design achieves the lowest delay of 0.032 ns and minimal power consumption of 0.335 µW with a reduced transistor count of 37. The XAC variant further reduces area to just 34 transistors, while maintaining efficient performance. These results confirm the effectiveness of the proposed architectures in advancing low-power, high-speed digital circuit design, making them highly suitable for next-generation VLSI systems.*

Keywords: VLSI design

DOI: 10.48175/IJARSCT-28813