

Design of CMOS Based two Stage Operational Amplifier with Improved Design Parameters for Both Inverting and Non-Inverting Functionality Mode

**Mr. G. D. Nagoshe, Mr. Soham R. Patil, Mr. Swapnil P. Karale,
Mr. Soham A. Holey, Mr. Vedant V. Raut**
Department of Electronics & Telecommunication
P. R. Pote (Patil) College of Engineering & Management, Amravati, India

Abstract: Operational amplifiers (op-amps) are fundamental components in analog and mixed-signal circuit design, with widespread applications in communication and medical systems. This project focuses on the design of a CMOS-based two-stage operational amplifier optimized for both inverting and non-inverting functionality. Utilizing 45 nm CMOS technology, the op-amp operates at a low supply voltage of 1V to reduce power dissipation. The design aims to achieve a high gain (≥ 60 dB), a unity gain bandwidth that meets or exceeds required specifications, and a phase margin of ≥ 45 degrees to ensure stability. Key parameters such as gain, bandwidth, slew rate, gain margin, and phase margin are carefully optimized to enhance performance. The design methodology strikes a balance between performance and power consumption, offering greater flexibility than previous approaches. The proposed op-amp is simulated and analyzed using Microwind EDA software. Simulation results indicate a power dissipation of 319.766 μ W and an occupied area of 10.9 μ m². The open loop gain is 20.18 dB, with a gain margin of 14.07 dB and a phase margin of 94.26°, ensuring unconditional stability. The op-amp's performance under dynamic conditions is verified through transient analysis, confirming its suitability for low-power applications. The design meets modern VLSI technology demands by optimizing parameters like power consumption and area, making it highly suitable for use in advanced analog systems.

Keywords: CMOS, Operational Amplifier (Op-Amp), Two-Stage Design, 45 nm Technology, Microwind EDA, Analog Circuit Design, VLSI Technology.

