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Design and Implementation of a MIPS Datapath

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Abstract: *Finally, the integration of these individual components culminates in the execution of the complete MIPS datapath. The MIPS (Microprocessor without Interlocked Pipeline Stages) architecture serves as a widely recognized and utilized instruction set architecture. Implementing the complete datapath involves orchestrating the flow of instructions through the CPU, from instruction fetch to execution and memory access, showcasing the culmination of our efforts in crafting a functional and efficient processor. In essence, this project not only provides a hands-on experience in HDL-based digital design but also immerses us in the intricacies of CPU architecture, emphasizing the importance of each component in achieving a harmonious and high-performance computing system..*

Keywords: MIPS, Computer Architecture, HDL Language, Computer Design, CPU

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