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Performance Evaluation of AMBA-3 AHB-Lite Protocol Verification: Techniques and Insights

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Abstract: *Verification is a crucial stage in SoC manufacturing so that the DUT has met specifications required by its user. It offers the DUT the specific implementation and functionality for the same purpose. The SoC design has the manufacturing capability, but it does not meet time to market requirements. The verification process, which looks into the right or wrong connection of the AHB LITE in the SoC design, has come out as one of the most strategic areas of concern in the design approach especially with increasing SoC designs. For instance, AMBA 3 AHB LITE is useful in SoC design that requires only one master, one or more slaves or several slaves. This paper discusses the AMBA 3 AHB-Lite protocol with more emphasis on design simulation and also the architecture of the testbench. AMBA in its first implementation presents two main buses, the "Advanced High-performance Bus (AHB)" for central control IPs and the "Advanced Peripheral Bus (APB)" for peripheral IPs. This paper focuses on the AHB-Lite subset as it is implemented to have high-bandwidth operations with a single bus master. It describes the features of AHB-Lite in terms of data transfer types and phases. The paper also expands on the verification environment of the AHB-Lite interconnects evaluating the testbench architecture, which encompasses the generators and master and slave agents and, drivers and scoreboards. The efficient creation of reusable testbenches and management of randomization is underscored by the Universal Verification Methodology (UVM). This paper shows how UVM helps to improve verification by finding corner cases and reporting coverage data. The paper concludes with an evaluation of simulation results, illustrating the effectiveness of the AHB-Lite protocol and its verification framework.*

Keywords: AHB-Lite, UVM, AMBA 3, Verification, SoC.APB

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