

# A Extensive Review of Recent Technologies and Trends in Low-Power VLSI Design

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**Abstract:** *The demand for energy-efficient electronic devices has driven significant advancements in low-power Very-Large-Scale Integration (VLSI) design. This paper presents a Extensive review of the recent technologies and trends that have emerged to address the challenges associated with power utilization in VLSI circuits. The review covers a broad spectrum of innovations, including advanced transistor technologies such as FinFETs, Gate-All-Around (GAA) FETs, and Silicon-on-Insulator (SOI), which offer improved power efficiency. It also explores cutting-edge power enhance techniques like Dynamic Voltage and Frequency Scaling (DVFS), power gating, and Multi-Threshold CMOS (MTCMOS), highlighting their impact on reducing both dynamic and leakage power. Further, the paper examines energy-efficient architectures, including Near-Threshold Computing (NTC), approximate computing, and asynchronous circuits, which promise substantial power savings. The fusing of machine learning and AI in power optimization and the development of advanced Electronic Design Automation tools are also discussed as emerging trends. Finally, the paper considers future directions, including the potential of 3D Integrated Circuits (3D ICs), quantum and neuromorphic computing, and post-CMOS technologies, to revolutionize low-power VLSI design. This review provides a critical exploration of the actual state of the art and offers comprehensions into the future trajectory of low-power VLSI, making it a valuable resource for researchers and practitioners in the field.*

**Keywords:** Low-Power Vlsi Design, DVFS, Power gating , Near-Threshold Computing, Machine Learning and AI