IJARSCT
ISSN (Online) 2581-9429
International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
Impact Factor: 7.53
Volume 4, Issue 2, August 2024

Implementation of 4-bit Universal Shift Register using Reversible Logic

Yathin[1], Shashank Pai[2], Nishma P Karkera[3], Sudheesha[4], Deepthi Shetty[5]
UG Students, Department of Electronics and Communication Engineering[1-4]
Senior Assistant Professor, Department of Electronics and Communication Engineering[5]
,Mangalore Institute of Technology & Engineering, Mangalore, India

Abstract: *The field of digital logic design is increasingly exploring reversible logic due to its potential in minimizing power dissipation, an essential criterion in low-power applications. This paper presents the design and implementation of a 4-bit universal shift register (USR) using reversible logic gates. The design leverages Fredkin gates, multiplexer (MUX), and D flip-flops to achieve functionality with minimal power consumption. Simulation results demonstrate the efficiency and effectiveness of the proposed design. Reversible logic is essential to low-power digital design and quantum computing because it makes it possible to reconstruct input signals from output signals, which reduces heat generation and information loss. The suggested shift register can be used for hold, parallel load, and left and right shift operations. To implement the functions of the shift register, we used a variety of reversible gates, including the Toffoli and Fredkin gates. When the architecture is contrasted with traditional non-reversible shift registers, it shows notable gains in reduced gate count and power efficiency*

Keywords: Reversible logic, Fredkin gate, universal shift register, multiplexer, D flip-flop, low power design