IJARSCT
ISSN (Online) 2581-9429
International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
Impact Factor: 7.53
Volume 4, Issue 2, July 2024

A Review on Implementation of Shift Register using FSM

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Abstract: *This study presents a way of decomposing Finite State Machines (FSMs) using shift registers as the memory for the FSM network components. Every part of the network is implemented using a different shift register. The FSM network's testability is enhanced by this method. The state splitting technique is explained in order to reduce the amount of shift registers that are used. In this implementation, every FSM state is defined to match a particular shift register configuration. Input signals and clock pulses control state transitions, guaranteeing precise data shifting from one stage to the next. The shifting, output, and initialization procedures are all included in the FSM architecture, which offers a comprehensible and upgradable structure for shift register operation.*

Keywords: Shift Register, Finite State Machine, Sequential Logic, Digital Circuit Design, Data Storage, Data Transfer, Flip-Flops