IJARSCT
International Journal of Advanced Research in Science, Communication and Technology
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
ISSN: 2581-9429
Volume 4, Issue 1, July 2024
Impact Factor: 7.53

Optimized Hybrid Flip-Flop with Conditional Boosting for Near-Threshold Voltage Applications

Mrs. Pabbala Priyanka[1], Dr. Sanju[2], Dr. M. Shashidhar[3]
Research Supervisor, Department of ECE[1]
Research Co Supervisor, Department of ECE[2]
NIILM University, Kaithal, Haryana, India[1,2]
Vaagdevi College of Engineering, Warangal, Telangana, India[3]
sasi47004@gmail.com

Abstract: *In addition to space and speed, the issue of power consumption is considered to be one of the challenges of modern VLSI design. The flip-flop forms part of digital systems. Four different flip-flop topologies in sub-threshold operation will be compared and contrasted, namely IP-DCO, MHLFF, CPSFF, and CPFF. Such topologies include conditional and pulse-triggered. Recently, it has become possible to apply applications with very low power consumption thanks to sub threshold technology. The advantage of this technology is that it makes the flip-flops consume less power. A subthreshold circuit consumes less power as compared to strong inversion circuit when the frequency is of the same frequency. Tanner uses the 18nm technology in cmos, design. The flip-flops are also tested at a power supply voltage of 1 V at various angles and the properties of the flip-flops such as average power, product of power delay, and power delay are measured.*

Keywords: Low-power, digital, design, efficiency, flip-flop, CMOS, energy-delay product, PVT variations