

# Specific Investigations Concerning the Improveable Multiplier Architecture of High-Speed and Area-Efficient Adders

Mayank Verma<sup>1</sup> and Anuradha Pathak<sup>2</sup>

PG Research Scholar, Embedded System and VLSI Design<sup>1</sup>

Assistant Professor, Embedded System and VLSI Design<sup>2</sup>

Nagaji Institute of Technology & Management, Gwalior, India

**Abstract:** *Over the past few decades, the growth of portable devices such as laptops, mobile phone and personal digital assistant has resulted in increasing demand for complex functionality with effective computation. The present day technology is known for digital systems with very high computing capabilities. The demand for high speed, low power integrated circuits for portable devices has become crucial. The never ending growing complexities of integrated circuit for future devices pose a challenging task for integrated circuit designer. Cost effective integrated circuits requires the design meeting out the challenging task to optimize power, area with high performance. Hence this research focuses on the optimization of area, power and speed of Arithmetic circuits, Very Large Scale Integrated circuits (VLSI) are widely used in Arithmetic circuits, Digital Signal Processing (DSP), Image and Video Processing applications*

**Keywords:** integrated circuits