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Design and Implementation of High Speed SRAM Cell

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Abstract: *Static Random Access Memory's main design goals are to have a consuming low power and high speed, as technology is developing at a faster paceand this has given rise to new challenges.The high speed along with stability of SRAM are important issues to improve efficiency and performance of the system. This proposed work presents design and implementation of 1Kb 6T SRAM using CMOS technologies by using EDA tool. In this proposed work, SRAM's cell is operated in 1V voltage. Our proposed high speed SRAM consisting 6T achieved read delay and write delay of 29.4ps & 15ps respectively. And also our designed cell has stability of 70 mV & 195 mV for read SNM and write SNM respectively.*

Keywords: Pre-charge, Row and Column Decoder, Sense Amplifier, Column mux and Write Driver

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