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Specific Design on Arithmetic Circuits with Low Power for VLSI Architectures

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Abstract: *The low power analog and digital systems are the major for any robotic applications. Designing low power and high-speed digital systems is one of the major and essential needs in VLSI Systems. Adder is the main key block in the digital systems. The entire digital systems performance is based on this adder block, which decides the overall power consumption and speed of the circuit. Various early designed full adder cell circuits encountered with low speed and high-power consumption issues. Here novel 1-bit full adder is designed based on XOR and XNOR Cell structure which operates in full swing and also the no critical path. With the use of three proposed the sum and carry is obtained. The main objective of this proposed full adder is to bring minimum power consumption and delay. The novel proposed full adder provides less power consumption by 94.68%, 90.82%, 84.54%, 35.61% and 83.43% while comparing with other full compared adders. The simulations were obtained in DSCH and Microwind tool*

Keywords: Full Adder design, XOR gate, XNOR gate, High speed, Robotics, Low power.

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