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FPGA Implementation of DFT Processor using Vedic Multiplier

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Abstract: *Many a times Mathematical computations are easier in frequency domain than time domain. Discrete Fourier transform (DFT) is a tool to convert signals from time domain to frequency domain which is widely used mainly in Digital Signal and ImageProcessing applications. Fast Fourier Transform (FFT) is a method to find DFT in time constraint applications which is affected by number of complex multiplier. In this paper 16-bit DFT using Vedic Multiplier, a high- speed multiplier is proposed with an objective to replace conventional complex multiplier and to decrease computation time. The proposed system is implemented in Virtex-4 FPGA and the results show that FFT using Urdhva Tiryakbhyam algorithm of Vedic multiplier is faster than other methods of DFT*

Keywords: Vedic Multiplier; Discrete FourierTransform; Fast Fourier Transform; Computational time

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