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Karatsubha Multiplier by using Verilog

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Abstract: *The Karatsuba multiplier is a widely-used algorithm that aims to efficiently multiply large numbers. Traditional multiplication algorithms have a time complexity of O(n^2), where n represents the number of digits in the input numbers. In contrast, the Karatsuba multiplier achieves a faster multiplication process by recursively splitting the numbers into smaller parts and performing intermediate multiplications using only three multiplications instead of four. This Modified architecture saves the 14.9% computation time and it consumes 45.5% less slices than existing Karatsuba multiplier. The proposed architecture has been simulated and synthesized by Xilinx vivado design suite for Spartan & Vertex device family. The new architecture is simple & easy. It emphasizes the significance of the Karatsuba multiplier in improving computational efficiency and highlights its implementation in different domains to accelerate large-scale multiplication tasks. Proposed hardware was implemented on different FPGA devices for various operand sizes, and performance parameters were determined. Comparing to state-of-theart works, the proposed method resulted in a lower combinational delay and area-delay product indicating the efficiency of design. In this we use two 32 bit inputs and produced the 64 bit as the output. In Spartan3E FPGA device family, Modified Karatsuba Algorithm (MKA) is 26.5% faster than Karatsuba Algorithm (KA).It consumes 61.7% less slices than existing KA based Convolution.*

Keywords: Crop recommendation, Humidity, Rainfall, pH, Machine Learning (ML), Random Forest (RF), Decision Tree (DT), Support Vector Machine (SVM), Logistic Regression (LR), and Naïve Bayes (NB),Data collection, Pre-processing, Feature extraction

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