Design of Smart Traffic Signal using Verilog

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Abstract: *Traffic light control can be designed as synchronous sequential machine with finite number of states. Explicit finite state model is used to design the necessary coding for control system using Verilog HDL. The machine is modeled with only six states necessary delay is provided and for that particular delay the necessary traffic lights are set ON and OFF. For illustration just only two roads Chosen and control algorithm controls the traffic lights of that roads proposes a flexible framework which provides a particular delaying particular using click divider, also discusses the issues of modeling the state machine in a synthes is friendly manner.*

The proposed system aims to optimize traffic flow and reduce congestion by dynamically adjusting signal timings based on real-time traffic data. The design includes modules for vehicle detection, data processing, and signal control. By utilizing Verilog's capabilities, the system achieves efficient and accurate signal management, enhancing over all traffic management and contributing to safer and more stream lined urban mobility..

Keywords: Verilog HDL

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