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Power Optimization Techniques in VLSI Circuits for Signal Processing Applications

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Abstract: *With the ever-growing demand for portable and energy-efficient electronic devices, power optimization in Very Large Scale Integration (VLSI) circuits has become a critical aspect of modern semiconductor design. This paper explores various power optimization techniques specifically tailored for VLSI circuits employed in signal processing applications. The study focuses on achieving a balance between high-performance signal processing and minimizing power consumption, a paramount concern in battery-powered and energy-constrained applications*

Keywords: Clock Gating, Power Gating, Low-Power Architectures

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