

International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)

International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal

Volume 4, Issue 2, May 2024

Ferro-Electric RAM

Vasanthamma. H¹, Lakhan Singh Rathore², Syed Sarfaraz Peer Hussaini³, Inayatulla⁴, Taralli Vijay⁵

Professor, Department of Computer Science and Engineering¹ Students, Department of Computer Science and Engineering^{2,3,4,5} Proudhadevaraya Institute of Technology, Hosapete, Karnataka, India

Abstract: Ferroelectric RAM (FRAM) is a promising non-volatile memory technology that combines the advantages of both DRAM and Flash memory. FRAM offers fast read and write speeds, low power consumption, and high endurance, making it suitable for a wide range of applications. It stores data by utilizing the ferroelectric properties of certain materials, which can retain their polarization even when the power is off. This allows FRAM to offer high-speed operation with low power consumption, making it ideal for use in IoT devices, smart cards, and automotive systems

Keywords: Ferroelectric RAM

I. INTRODUCTION

1.1 Definition

Ferromagnetic cores were the only type of random-access, non-volatile memories available. A core memory is a regular array of tiny magnetic cores that can be magnetized in one of two opposite directions, making it possible to store binary data in the form of a magnetic field.

A ferroelectric capacitor is different from a regular capacitor in that it substitutes the dielectric with a ferroelectric material (lead zirconate titanate (PZT) is a common material used)-when an electric field is applied and the charges displace from their original position spontaneous polarization occurs and displacement becomes evident in the crystal structure of the material.

A ferroelectric memory cell has at least one ferroelectric capacitor to store the binary data, and one transistor that provides access to the capacitor or amplifies its content for a read operation. Once a cell is accessed for a read operation, its data are presented in the form of an analog signal to a sense amplifier, where they are compared against a reference voltage to determine their logic level.

1.2 Problem Statement

Increasing demand for high-performance, low-power non-volatile memory solutions has highlighted the need for advancements in RAM technology. Current RAM implementations face challenges related to scalability, endurance, and writing speed, limiting their widespread adoption in modern electronic devices. Addressing these challenges is crucial to unlock the full potential of RAM as a reliable, high-speed, non-volatile memory alternative to existing technologies.

1.3 Objectives

- Ferro-Electric RAM(FRAM) is non-volatile, meaning it retains data even when power is removed. This property makes FRAM suitable for applications requiring instant-on or persistent data storage without the need for battery backup.
- FRAM offers fast read and write speeds compared to traditional non-volatile memory technologies like Flash. This makes FRAM ideal for applications requiring frequent read/write operations or low-latency data access.
- RAM consumes less power compared to other non-volatile memory technologies, making it suitable for battery-powered devices or applications where power efficiency is critical.
- FRAM has high endurance, meaning it can withstand a large number of read and write cycles without degradation. This makes FRAM suitable for applications requiring frequent data updates.

Copyright to IJARSCT www.ijarsct.co.in DOI: 10.48175/IJARSCT-18128





International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)

International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal

Volume 4, Issue 2, May 2024

- FRAM is available in compact chip sizes, making it suitable for use in small form factor devices or applications where space is limited.
- FRAM can be easily integrated into existing semiconductor manufacturing processes, making it a costeffective solution for many applications.

II. METHODOLOGY

2.1 Components

Cell Structure:

The basic unit of FeRAM is the memory cell, which consists of a ferroelectric capacitor and a transistor. The ferroelectric capacitor stores the data, while the transistor acts as a switch to read and write data to the capacitor.

Ferro-electric Layer:

The ferroelectric layer is made of a material that can switch polarization when an electric field is applied. This allows the material to store data polarization states, representing binary values (0 and 1).

Transistor:

Each memory cell is accessed through a transistor, typically a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor). The transistor controls the flow of current to the ferroelectric capacitor, enabling the read and write operations.

Word and Bit Lines:

FeRAM uses word lines and bit lines to address individual memory cells. The word lines select a row of memory cells, while the bit lines select a specific cell within the row for read or write operations.

Sense Amplifiers:

Sense amplifiers are used to detect the polarization state of the ferroelectric capacitor during a read operation. The sense amplifiers amplify the small signal from the capacitor to a level that can be interpreted as a logic '0' or '1'.

Decoders and Multiplexers:

Decoders and multiplexers are used to select the appropriate word and bit lines for accessing memory cells, based on the address provided by the memory controller.

Control Logic:

The control logic coordinates the read and write operations, ensuring that data is correctly stored and retrieved from the memory cells.

2.2 Architecture



Copyright to IJARSCT www.ijarsct.co.in



International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)

International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal

Volume 4, Issue 2, May 2024

2.3 Methodology

The cell consists of a single ferroelectric capacitor that is connected to a PL at one end and via an access transistor, to a BL at the other end. The cell is accessed by raising the wordline (WL) and hence turning ON the access transistor. The access is one of two types: a write access or a read access.

Write Operation:

- The FRAM device activates the row decoder circuitry based on the row address received from the memory controller, enabling the selected row for writing.
- The memory controller sends the address of the target memory cell to the FRAM device, specifying the row and column of the cell.
- A write voltage is applied to the selected row, creating an electric field across the ferroelectric material in the target cell. This electric field causes the polarization of the ferroelectric material to switch to the desired state, representing the data to be written.
- The ferroelectric material in the target cell switches its polarization direction in response to the applied electric field. This switch is facilitated by the ferroelectric material's property of having multiple stable polarization states.
- After the write voltage is applied and removed, the sense amplifiers in the FRAM device detect the polarization state of the ferroelectric material in the target cell to confirm that the write operation was successful.
- The polarization state of the ferroelectric material stabilizes over time, ensuring that the data remains stored even after the write voltage is removed.



Fig.2. Read/Write operations in a FE-RAM

Read Operation:

- The read operation of Ferroelectric RAM (FRAM) involves sensing the polarization state of the ferroelectric material to determine the stored data.
- The memory controller activates the row and column lines corresponding to the target cell, enabling access to that specific cell.
- To read data from a specific memory cell in an FRAM array, the address of the cell is provided to the memory controller.
- A read voltage is applied to the selected cell, causing the polarization of the ferroelectric material to switch if it was in the opposite state. This switching generates a small current or voltage, which is sensed by the memory controller.

Copyright to IJARSCT www.ijarsct.co.in

DOI: 10.48175/IJARSCT-18128





International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)

International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal

Volume 4, Issue 2, May 2024

- Based on the sensed current or voltage, the memory controller determines the stored data. For example, if a high current is sensed, it indicates a logic "1," while a low current indicates a logic "0."
- In some cases, especially for high-density FRAM devices, the read operation may be followed by a refresh operation. This is done to ensure that the polarization state of the ferroelectric material is maintained over time, as it can gradually degrade due to leakage currents.

III. COMPARISON BETWEEN FE-RAM AND OTHER RAM MEMORIES

FE-RAM v/s DRAM:

- FeRAM retains data even when power is removed, similar to non-volatile memory like Flash. DRAM requires power to maintain data, so it is volatile.
- FeRAM has a fast write speed, comparable to SRAM, and is much faster than DRAM. DRAM has slower write speeds due to its design.
- FeRAM has a high endurance, with the ability to withstand millions to billions of write cycles. DRAM, on the other hand, has limited endurance due to its design, which involves constant refreshing of the stored data.
- FeRAM typically consumes less power than DRAM because it does not require constant refreshing. However, it may consume more power than non-volatile memories like Flash.
- DRAM can achieve higher densities and capacities compared to FeRAM. This is why DRAM is commonly used for main memory in computers.
- FeRAM is generally more expensive than DRAM, which limits its use in certain applications.

FE-RAM v/s SRAM:

- FeRAM retains data even when power is removed, similar to non-volatile memory like Flash. SRAM is volatile and requires power to maintain data.
- FeRAM has a fast write speed, comparable to SRAM, and is much faster than DRAM. Both FeRAM and SRAM have faster write speeds than DRAM.
- FeRAM has a high endurance, with the ability to withstand millions to billions of write cycles. SRAM, on the other hand, is typically not designed for high endurance applications.
- FeRAM typically consumes less power than SRAM because it does not require constant refreshing. However, SRAM's power consumption is lower than DRAM.
- SRAM can achieve higher densities and capacities compared to FeRAM. This is why SRAM is commonly used for cache memory in computers.
- FeRAM is generally more expensive than SRAM, which limits its use in certain applications.

FE-RAM v/s Flash Memory:

- FeRAM retains data even when power is removed, similar to Flash memory. However, FeRAM typically has a higher endurance and can withstand more write cycles than Flash memory.
- FeRAM has a fast write speed, similar to SRAM, and is much faster than Flash memory. Flash memory has slower write speeds compared to FeRAM.
- FeRAM has a high endurance, with the ability to withstand millions to billions of write cycles. Flash memory, while offering good endurance, has a limited number of write cycles, typically in the range of thousands to hundreds of thousands.
- FeRAM typically consumes less power than Flash memory because it does not require high voltage programming operations. However, Flash memory has lower power consumption compared to many other non-volatile memory technologies.
- Flash memory can achieve higher densities and capacities compared to FeRAM. This is why Flash memory is commonly used for mass storage in devices like USB drives, SSDs, and memory cards.
- FeRAM is generally more expensive than Flash memory, which limits its use in certain applications where cost is a critical factor.

DOI: 10.48175/IJARSCT-18128





International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)

International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal

Volume 4, Issue 2, May 2024

TABLE I: Comparison Between FE-RAM and Other RAM Memories

	FRAM	Flash Memory	DRAM	SRAM
Memory Type	Non-Volatile	Non-Volatile	Volatile	Volatile
Read Cycle	100ns	120ns	70ns	85ns
Write Cycle	100ns	100us	70ns	85ns
Power Consumption	lnJ	2uJ	4uJ	3uJ
Current to Retain Data	Unnecessary	Unnecessary	Necessary	Necessary
Internal Write Voltage	2V-5V	9V	3.3V	3.3V
Cell Structure	IT-IC	IT	IT-IC	6T,4T+R

IV. EXPECTED OUTCOMES

- FRAM offers faster read and write speeds compared to traditional non-volatile memory technologies like Flash memory.
- FRAM consumes less power compared to other non-volatile memory technologies, making it suitable for battery-powered devices or applications where power efficiency is critical.
- FRAM has high endurance, meaning it can withstand a large number of read and write cycles without degradation. This can result in increased reliability and longer lifespan for devices using FRAM.
- FRAM is non-volatile, meaning it retains data even when power is removed. This allows devices to resume operation instantly without the need for lengthy boot-up sequences, improving user experience.

V. CONCLUSION

Ferroelectric RAM (FeRAM) is a promising non-volatile memory technology with several advantages, including fast read and write speeds, low power consumption, high endurance, and non-volatile data retention. FeRAM is a valuable memory technology that continues to see advancements and improvements, making it a compelling choice for applications where fast, reliable, and low-power non-volatile memory is required.

REFERENCES

[1]. S. Fujisaki, H. Ishiwara, and Y. Fujisaki, Appl. Phys. Lett. 90, 162902 (2007).

[2]. T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, Appl. Phys. Lett. 99, 102903 (2011).

[3]. Y. Arimoto and H. Ishiwara, MRS Bulletin 29, 823 (2004).

[4]. C.-Y. Koo, J.-H. Cheon, J.-H. Yeom, J. Ha, S.-H. Kim, and S.-K.Hong, J. Korean Phys. Soc. 49, S514 (2006).

[5]. M.-H. Tang, G.-J. Dong, Y. Sugiyama, and H. Ishiwara, Semicond.Sci. Technol. 25, 035006 (2010).

[6]. J. Wang, J. B. Neaton, H. Zheng, V. Nagarajan, S. B. Ogale, B. Liu, D. Viehland, V. Vaithyanathan, D. G. Schlom,

U. V. Waghmare, N. A. Spaldin, K. M. Rabe, M. Wuttig, and R. Ramesh, Science299, 1719 (2003).

[7]. H. Ishiwara, Curr. Appl. Phys. 12, 603 (2012).

[8]. Y. H. Chu, Q. Zhan, C.-H. Yang, M. P. Cruz, L. W. Martin, T. Zhao, P. Yu, R. Ramesh, P. T. Joseph, I. N. Lin, W. Tian, and D. G. Schlom, Appl. Phys. Lett. 92, 102909 (2008).

[9]. S. K. Singh, H. Ishiwara, and K. Maruyama, Appl. Phys. Lett.88, 262908 (2006).

[10]. S. Masui, T. Ninomiya, T. Ohkawa, M. Oura, Y. Horii, N. Kin, and K. Honda, IEICE Trans. Electron. E87-C, 1769 (2004).

[11]. H. Ishiwara, Curr. Appl. Phys. 9, S2 (2009).

[12]. S. Sakai and R. Ilangovan, IEEE Electron Device Lett. 25, 369(2004).

[13]. K. Takahashi, K. Aizawa, B.-E. Park, and H. Ishiwara, Jpn. J. Appl. Phys. 44, 6218 (2005).

[14]. Q.-H. Li and S. Sakai, Appl. Phys. Lett. 89, 222910 (2006).

[15]. H. Ishiwara, T. Shimamura, and E. Tokumitsu, Jpn. J. Appl. Phys. 36, 1655 (1997).

Copyright to IJARSCT www.ijarsct.co.in DOI: 10.48175/IJARSCT-18128



186



International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)

International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal

Volume 4, Issue 2, May 2024

[16]. T. Hatanaka, R. Yajima, T. Horiuchi, S. Wang, X. Zhang, M. Takahashi, S. Sakai, and K. Takeuchi, IEEE J. Solid-StateCircuits 45, 2156 (2010).

[17]. X. Zhang, M. Takahashi, K. Takeuchi, and S. Sakai, Abstract ofIntern. Conf. on Solid State Devices and Materials, Nagoya, F-3-1(2011).

