IJARSCT
ISSN (Online) 2581-9429
International Journal of Advanced Research in Science, Communication and Technology (IJARSCT)
International Open-Access, Double-Blind, Peer-Reviewed, Refereed, Multidisciplinary Online Journal
Impact Factor: 7.53
Volume 4, Issue 2, May 2024

An Efficient Design of 2-BIT Arithmetic Logical Unit in Quantum Dot Cellular Automata

Gaurang Tyagi, Sadhana Kumari, Ayushi Ojha, Shivanshu Nanda
Department of Electronic and Communication Engineering
JSS Academy of Technical Education, Noida, (U.P), India
gaurangtyagi19@gmail.com, sadhana.kumari@jssaten.ac.in, ayushiojha1012@gmail.com, shivanshun33@gmail.com

Abstract: *For the past two decades, CMOS technology has reigned supreme in the world of Very Large Scale Integration (VLSI). But Quantum Dot Cellular Automata (QCA) is stepping into the spotlight, offering a fresh solution to the growing challenges of CMOS. This paper delves into the potential of QCA circuits by presenting a 2-bit Arithmetic Logic Unit (ALU) crafted with this groundbreaking technology, while also benchmarking it against conventional CMOS designs. The proposed QCA-based ALU delivers a trifecta of benefits: streamlined circuit design, exceptional space efficiency, and reduced quantum cost—all while keeping performance sharp in terms of latency and area usage. This 2-bit ALU encompasses a suite of operations: addition, subtraction, multiplication, division, bitwise AND, OR, XOR, and XNOR. QCA technology addresses some of CMOS's major pain points, like slow switching speeds, and doesn't require additional power sources, making it both efficient and environmentally friendly. This is not just an incremental improvement; it's a bold leap into the future of circuit design*

Keywords: Clock Signal; Adder; Subtractor; Multiplier; Switching Speed; Demultiplexer

DOI: 10.48175/IJARSCT-18128